This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A feedforward amplifier comprising:

a first power splitter for splitting an input signal into two parts;

a first vector adjustor for adjusting the amplitude and phase of one output signal of said first power splitter;

a main amplifier for amplifying an output signal of said first vector adjustor;

a second power splitter for splitting an output signal of said main amplifier into two parts;

a first delay circuit for delaying the other output signal of said first power splitter;

a distortion detection power-combiner for synthesizing one output signal of said second power splitter and an output signal of said first delay circuit;

a second delay circuit for delaying the other output signal of said second power splitter;

a second vector adjustor for adjusting the amplitude and phase of the output signal of said distortion detection power-combiner;

an error amplifier for amplifying the output signal of said second vector adjustor;

a distortion suppression power-combiner for synthesizing the output signal of said second delay circuit and the output signal of said error amplifier; ~~and~~

control means of at least stopping the operation of said error amplifier or said main amplifier depending on a predetermined condition;

first signal level detection means of detecting a first signal level that is the signal level of said input signal, or the signal level of a baseband signal in a baseband signal generating portion, or the signal level of a transmitting signal in a transmitting circuit, or the signal level of a received signal in a receiving circuit; and

second signal level detection means of detecting a second signal level that is the signal level of said output signal,

wherein said predetermined condition represents gain of said second signal level to said first signal level, and

when said gain is out of a predetermined value, said control means stops the operation of said main amplifier.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) The feedforward amplifier according to claim ~~4 or 5~~1, wherein said distortion suppression power-combiner is a variable power-combiner that can have a tight coupling state and a loose coupling state, and

when said first signal level is higher than a predetermined value, said control means controls said variable power-combiner to have said loose coupling state, and

when said first signal level is not higher than the predetermined value, said control means controls said variable power-combiner to have said tight coupling state.

8. (Currently Amended) The feedforward amplifier according to claim ~~4 or 6~~1, wherein said distortion suppression power-combiner is a variable power-combiner that can have a tight coupling state and a loose coupling state,

when said first signal level is lower than a predetermined value, said control means controls said variable power-combiner to have said loose coupling state, and

when said first signal level is not lower than the predetermined value, said control means controls said variable power-combiner to have said tight coupling state.

9. (Currently Amended) The feedforward amplifier according to claim ~~4 or 5~~1, wherein, when said first signal level is not higher than a predetermined value, said control means performs such control that the output signal of said error amplifier can be output without passing through said distortion suppression power-combiner.

10. (Currently Amended) The feedforward amplifier according to claim ~~4 or 6~~1, wherein, when said first signal level is not lower than a predetermined value, said control means performs such control that the output signal of said error amplifier can be output without passing through said distortion suppression power-combiner.

11. (Cancelled)

12. (Cancelled)

13. (Currently Amended) ~~The~~A feedforward amplifier ~~according to claim 1, further~~ comprising:

a first power splitter for splitting an input signal into two parts;

a first vector adjustor for adjusting the amplitude and phase of one output signal of said first power splitter;

a main amplifier for amplifying an output signal of said first vector adjustor;

a second power splitter for splitting an output signal of said main amplifier into two parts;

a first delay circuit for delaying the other output signal of said first power splitter;

a distortion detection power-combiner for synthesizing one output signal of said second power splitter and an output signal of said first delay circuit;

a second delay circuit for delaying the other output signal of said second power splitter;

a second vector adjustor for adjusting the amplitude and phase of the output signal of said distortion detection power-combiner;

an error amplifier for amplifying the output signal of said second vector adjustor;

a distortion suppression power-combiner for synthesizing the output signal of said second delay circuit and the output signal of said error amplifier;

control means of at least stopping the operation of said error amplifier or said main amplifier depending on a predetermined condition;

a third power splitter for splitting the output signal of said error amplifier into two parts;

a third delay circuit for delaying one output signal of said third power splitter;

a fourth power splitter for splitting the output signal of said distortion suppression power-combiner into two parts;

a fourth delay circuit for delaying one output signal of said fourth power splitter;

a second distortion detection power-combiner for synthesizing the output signal of said fourth delay circuit and the other output signal of said third power splitter;

a third vector adjustor for adjusting the amplitude and phase of the output signal of said second distortion detection power-combiner;

a second error amplifier for amplifying the output signal of said third vector adjustor;

a second distortion suppression power-combiner for synthesizing the output signal of said third delay circuit and the output signal of said second error amplifier; and

first signal level detection means of detecting a first signal level that is the signal level of said input signal, or the signal level of a baseband signal in a baseband signal generating portion, or the signal of a transmitting signal in a transmitting circuit,

wherein said control means also stops the operation of said second error amplifier depending on said predetermined condition,

said predetermined condition represents said first signal level, and

when said first signal level is higher than a predetermined value, said control means stops the operation of said second error amplifier and performs such control that the output signal of said error amplifier can not be input by said third power splitter, and performs such control that the output signal of said distortion suppression power-combiner can be output to the outside, and

when said first signal level is not higher than the predetermined value, said control means stops the operation of said main amplifier and performs such control that the output signal of said error amplifier can not be input by said distortion suppression power-combiner but can be input by said third power splitter, and performs such control that the output signal of said second distortion suppression power-combiner can be output to the outside.

14. (Currently Amended) ~~The~~A feedforward amplifier ~~according to claim 1, further~~ comprising:

a first power splitter for splitting an input signal into two parts;

a first vector adjustor for adjusting the amplitude and phase of one output signal of said first power splitter;

a main amplifier for amplifying an output signal of said first vector adjustor;

a second power splitter for splitting an output signal of said main amplifier into two parts;

a first delay circuit for delaying the other output signal of said first power splitter;

a distortion detection power-combiner for synthesizing one output signal of said second power splitter and an output signal of said first delay circuit;

a second delay circuit for delaying the other output signal of said second power splitter;

a second vector adjustor for adjusting the amplitude and phase of the output signal of said distortion detection power-combiner;

an error amplifier for amplifying the output signal of said second vector adjustor;

a distortion suppression power-combiner for synthesizing the output signal of said second delay circuit and the output signal of said error amplifier;

control means of at least stopping the operation of said error amplifier or said main amplifier depending on a predetermined condition;

a third power splitter for splitting the output signal of said error amplifier into two parts;

a third delay circuit for delaying one output signal of said third power splitter;

a fourth power splitter for splitting the output signal of said distortion suppression power-combiner into two parts;

a fourth delay circuit for delaying one output signal of said fourth power splitter;

a second distortion detection power-combiner for synthesizing the output signal of said fourth delay circuit and the other output signal of said third power splitter;

a third vector adjustor for adjusting the amplitude and phase of the output signal of said second distortion detection power-combiner;

a second error amplifier for amplifying the output signal of said third vector adjustor;

a second distortion suppression power-combiner for synthesizing the output signal of said third delay circuit and the output signal of said second error amplifier; and

first signal level detection means of detecting a first signal level that is the signal level of a received signal in a receiving circuit,

wherein said control means also stops the operation of said second error amplifier depending on said predetermined condition,

said predetermined condition represents said first signal level, and

when said first signal level is lower than a predetermined value, said control means stops the operation of said second error amplifier and performs such control that the output signal of said error amplifier can not be input by said third power splitter, and performs such control that the output signal of said distortion suppression power-combiner can be output to the outside, and

when said first signal level is not lower than the predetermined value, said control means stops the operation of said main amplifier and performs such control that the output signal of said error amplifier can not be input by said distortion suppression power-combiner but can be input by said third power splitter, and performs such control that the output signal of said second distortion suppression power-combiner can be output to the outside.

15. (Currently Amended) ~~The~~A feedforward amplifier ~~according to claim 1, further~~ comprising:

a first power splitter for splitting an input signal into two parts;

a first vector adjustor for adjusting the amplitude and phase of one output signal of said first power splitter;

a main amplifier for amplifying an output signal of said first vector adjustor;

a second power splitter for splitting an output signal of said main amplifier into two parts;

a first delay circuit for delaying the other output signal of said first power splitter;

a distortion detection power-combiner for synthesizing one output signal of said second power splitter and an output signal of said first delay circuit;

a second delay circuit for delaying the other output signal of said second power splitter;

a second vector adjustor for adjusting the amplitude and phase of the output signal of said distortion detection power-combiner;

an error amplifier for amplifying the output signal of said second vector adjustor;

a distortion suppression power-combiner for synthesizing the output signal of said second delay circuit and the output signal of said error amplifier;

control means of at least stopping the operation of said error amplifier or said main amplifier depending on a predetermined condition;

a third power splitter for splitting the output signal of said error amplifier into two parts;

a third delay circuit for delaying one output signal of said third power splitter;

a fourth power splitter for splitting the output signal of said distortion suppression power-combiner into two parts;

a fourth delay circuit for delaying one output signal of said fourth power splitter;

a second distortion detection power-combiner for synthesizing the output signal of said fourth delay circuit and the other output signal of said third power splitter;

a third vector adjustor for adjusting the amplitude and phase of the output signal of said second distortion detection power-combiner;

a second error amplifier for amplifying the output signal of said third vector adjustor;

a second distortion suppression power-combiner for synthesizing the output signal of said third delay circuit and the output signal of said second error amplifier; and

first signal level detection means of detecting a first signal level that is the signal level of said input signal, or the signal level of a baseband signal in a baseband signal generating portion, or the signal of a transmitting signal in a transmitting circuit,

wherein said control means also stops the operation of said second error amplifier depending on said predetermined condition,

said predetermined condition represents said first signal level, and

when said first signal level is higher than a predetermined value, said control means stops the operation of said second error amplifier and performs such control that the output signal of said error amplifier can not be input by said third power splitter, and performs such control that the output signal of said distortion suppression power-combiner can be output to the outside, and

when said first signal level is not higher than the first predetermined value and higher than a second predetermined value that is smaller than said first predetermined value, said control means stops the operation of said main amplifier

and performs such control that the output signal of said error amplifier can not be input by said distortion suppression power-combiner but can be input by said third power splitter, and performs such control that the output signal of said second distortion suppression power-combiner can be output to the outside, and

when said first signal level is not higher than the second predetermined value, said control means stops the operation of said error amplifier and stops the operation of said second error amplifier, and performs such control that the output signal of said distortion suppression power-combiner can be output to the outside.

16. (Currently Amended) ~~The~~A feedforward amplifier ~~according to claim 1, further~~ comprising:

a first power splitter for splitting an input signal into two parts;

a first vector adjustor for adjusting the amplitude and phase of one output signal of said first power splitter;

a main amplifier for amplifying an output signal of said first vector adjustor;

a second power splitter for splitting an output signal of said main amplifier into two parts;

a first delay circuit for delaying the other output signal of said first power splitter;

a distortion detection power-combiner for synthesizing one output signal of said second power splitter and an output signal of said first delay circuit;

a second delay circuit for delaying the other output signal of said second power splitter;

a second vector adjustor for adjusting the amplitude and phase of the output signal of said distortion detection power-combiner;

an error amplifier for amplifying the output signal of said second vector adjustor;

a distortion suppression power-combiner for synthesizing the output signal of said second delay circuit and the output signal of said error amplifier;

control means of at least stopping the operation of said error amplifier or said main amplifier depending on a predetermined condition;

a third power splitter for splitting the output signal of said error amplifier into two parts;

a third delay circuit for delaying one output signal of said third power splitter;

a fourth power splitter for splitting the output signal of said distortion suppression power-combiner into two parts;

a fourth delay circuit for delaying one output signal of said fourth power splitter;

a second distortion detection power-combiner for synthesizing the output signal of said fourth delay circuit and the other output signal of said third power splitter;

a third vector adjustor for adjusting the amplitude and phase of the output signal of said second distortion detection power-combiner;

a second error amplifier for amplifying the output signal of said third vector adjustor;

a second distortion suppression power-combiner for synthesizing the output signal of said third delay circuit and the output signal of said second error amplifier; and

first signal level detection means of detecting a first signal level that is the signal level of a received signal in a receiving circuit,

wherein said control means also stops the operation of said second error amplifier depending on said predetermined condition,

said predetermined condition represents said first signal level, and

when said first signal level is lower than a second predetermined value, said control means stops the operation of said second error amplifier and performs such control that the output signal of said error amplifier can not be input by said third power splitter, and performs such control that the output signal of said distortion suppression power-combiner can be output to the outside, and

when said first signal level is not higher than a first predetermined value that is larger than said second predetermined value and higher than said second predetermined value, said control means stops the operation of said main amplifier and performs such control that the output signal of said error amplifier can not be input by said distortion suppression power-combiner but can be input by said third power splitter, and performs such control that the output signal of said second distortion suppression power-combiner can be output to the outside, and

when said first signal level is not lower than the first predetermined value, said control means stops the operation of said error amplifier and stops the operation of said second error amplifier, and performs such control that the output signal of said distortion suppression power-combiner can be output to the outside.

17. (Currently Amended) The feedforward amplifier according to any one of claims ~~2, 4, 5, 11,~~ 1, 13, and 15, wherein said first signal level detection means is provided in an upstream stage of said first power splitter, or between said first power splitter and said first vector adjustor, or between said first vector adjustor and said main amplifier, or between said first power splitter and said first delay circuit, or between said first delay circuit and said distortion detection power-combiner, or at the input of said baseband signal generating portion, or at the output of said baseband signal generating portion, or in said baseband signal generating potion, or at the input of said transmitting circuit, or at the output of said transmitting circuit, or in said transmitting circuit.

18. (Currently Amended) The feedback amplifier according to any one of claims ~~3, 4, 6, 12,~~ 1, 14, and 16, wherein said first signal level detection means is provided at the input of said receiving circuit, or at the output of said receiving circuit, or in said receiving circuit.

19. (Currently Amended) The feedforward amplifier according to claim 1, ~~4,~~ wherein said second signal level detection means is provided in a downstream stage of said distortion suppression power-combiner, or between said second power splitter and said second delay circuit, or between said second delay circuit and said distortion suppression power-combiner.

20. (Original) The feedforward amplifier according to claim 17,

wherein said first signal level is the signal level of said input signal, and when said first signal level detection means detects the signal level of said input signal,

said first signal level detection means has a signal level detection power-splitter for splitting said input signal into two parts and detection means of detecting said signal level of one output signal of said signal level detection power-splitter, and

the other output signal of said signal level detection power splitter is supplied to a downstream stage.

21. (Original) The feedforward amplifier according to claim 19, wherein said second signal level detection means has a signal level detection power-splitter for splitting said output signal into two parts and detection means of detecting said signal level of one output signal of said signal level detection power-splitter, and

the other output signal of said signal level detection power-splitter is supplied to a downstream stage.

22. (Currently Amended) The feedforward amplifier according to any one of claims ~~2, 3, 11, 12,~~ 15~~,~~ and 16, wherein the stopping of the operation of said error amplifier is to perform such control that the power supply for said error amplifier can be turned off and/or to perform such control that the output signal of said second vector adjustor can not be input by said error amplifier.

23. (Currently Amended) The feedforward amplifier according to any one of claims ~~4, 5, 6, 11, 12,~~ 1, 13, 14, 15, and 16, wherein the stopping of the operation of said main amplifier is to perform such control that the power supply for said main

amplifier can be turned off and/or to perform such control that the output signal of said first vector adjustor can not be input by said main amplifier.

24. (Original) The feedforward amplifier according to any one of claims 13, 14, 15, and 16, wherein the stopping of the operation of said second error amplifier is to perform such control that the power supply for said second error amplifier can be turned off and/or to perform such control that the output signal of said third vector adjustor can not be input by said secondary error amplifier.

25. (Currently Amended) A communication equipment comprising:

a baseband generating portion for generating a baseband signal; and

a transmitting circuit for outputting a transmitting signal from said baseband signal generated, wherein the feedforward amplifier according to any one of claims 1 ~~to 3, 5 to 6~~, ~~11~~ 13 to 16, 19, and 21 is used for said transmitting circuit.